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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/788,683	DO ET AL.
	Examiner	Art Unit
	Quan Tra	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/06/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 5, 7, 9-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Ikehashi et al. (USP 6642757).

As to claim 1, Ikehashi et al. discloses in figure 23 a power-up circuit comprising: a power supply voltage level follower unit (the three series connected resistors) outputting a first bias voltage and a second bias voltage (at nodes between the resistors) which increase or decrease in proportion to a power supply voltage; a first power supply voltage detecting unit (circuit having the N-channel transistor connected in series with the depletion transistor and the resistor) for detecting that the power supply voltage becomes a first critical voltage level of the power supply voltage corresponding to a threshold voltage of an NMOS transistor in response to the first bias voltage; a second power supply voltage detecting unit (circuit having the P-channel transistor connected in series with the depletion transistor and the resistor) for detecting that the power supply voltage becomes a second critical voltage level of the power supply voltage corresponding to a threshold voltage of a PMOS transistor in response to the second bias voltage; and a summation unit (the NAND gate) for performing a logic operation to a first detect signal

outputted from the first power supply voltage detecting unit and a second detect signal outputted from the second power supply voltage detecting unit to thereby output a confirmation signal, wherein the confirmation signal is activated when the power supply voltage satisfies both of the first and second critical voltage levels.

As to claim 2, figure 23 further shows a buffering unit (the inverters connected to the output of the NAND gate) for buffering the confirmation signal outputted from the summation unit to thereby output a power-up signal.

As to claim 3, figure 23 shows that the power supply voltage level follower unit includes a first load element (the highest resistor), a second load element (the middle resistor) and a third load element (the lowest resistor), all connected between the power supply voltage and a ground voltage in series, for outputting the first bias voltage to a first common node between the first load element and the second load element and outputting the second bias voltage to a second common node between the second load element and the third load element.

As to claim 5, figure 23 shows that the first power supply voltage detecting unit includes: a first load element (the resistor) connected between the power supply voltage and a first node; an NMOS transistor (the N-channel transistor) connected between the first node and a ground voltage for receiving the first bias voltage through a gate of the NMOS transistor; and a first inverter connected to the first node (as shown).

As to claim 7, figure 23 shows that the second power supply voltage detecting unit includes: a second load element (the resistor) connected between the ground voltage and a second node; a PMOS transistor connected between the second node and the power supply voltage for receiving the second bias voltage through a gate of the PMOS transistor;

a second inverter connected to the second node; and a third inverter for receiving an outputted signal from the second inverter.

As to claim 9, figure 23 shows that the summation unit includes: a NAND gate for receiving the first detect signal and the second detect signal; and a fourth inverter for receiving an outputted signal from the NAND gate.

As to claim 10, figure 23 shows that the summation unit includes a NOR gate (the circuit that comprises the NAND gate, the two inverter that directly connected to the inputs the NAND gate, and the inverter that directly connected to the output of the NAND gate functions as a NOR gate) of for receiving the first detect signal and the second detect signal.

As to claim 11, figure 23 shows that the buffering unit includes buffers (inverters) connected serial for receiving the confirmation signal.

3. Claims 1, 2, 4, 5, 9, 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Onishi (JP 2001-127609).

As to claim 1, Onishi discloses in figure 1 a power-up circuit comprising: a power supply voltage level follower unit (R11-Rh1 and R14-Rh2) outputting a first bias voltage and a second bias voltage (at node between R11 and R12 and node between R14 and R15) which increase or decrease in proportion to a power supply voltage; a first power supply voltage detecting unit (the remaining elements in circuit 1) for detecting that the power supply voltage becomes a first critical voltage level of the power supply voltage corresponding to a threshold voltage of an NMOS transistor (N2) in response to the first bias voltage; a second power supply voltage detecting unit (the remaining elements in circuit 2) for detecting that the power supply voltage becomes a second critical voltage level of the power supply voltage corresponding to a threshold

voltage of a PMOS transistor (P2) in response to the second bias voltage; and a summation unit (3) for performing a logic operation to a first detect signal outputted from the first power supply voltage detecting unit and a second detect signal outputted from the second power supply voltage detecting unit to thereby output a confirmation signal, wherein the confirmation signal is activated when the power supply voltage satisfies both of the first and second critical voltage levels.

As to claim 2, figure 1 further shows a buffering unit (4) for buffering the confirmation signal outputted from the summation unit to thereby output a power-up signal.

As to claim 4, figure 1 shows that the power supply voltage level follower unit includes: a first power supply voltage level follower unit (R11, R12, Rh1) having a first load element (R11) and a second load element (R12) connected series between the power supply voltage and a ground voltage; and a second power supply voltage level follower (R14, R15, Rh2) unit having a third load element (R14) and a fourth load element (R15) connected in series between the power supply voltage and the ground voltage.

As to claim 5, figure 1 shows that the first power supply voltage detecting unit includes: a first load element (R13) connected between the power supply voltage and a first node; an NMOS transistor (N2) connected between the first node and a ground voltage for receiving the first bias voltage through a gate of the NMOS transistor; and a first inverter (10) connected to the first node.

As to claim 9, figure 1 shows that the summation unit includes: a NAND gate for receiving the first detect signal and the second detect signal; and a fourth inverter for receiving an outputted signal from the NAND gate.

As to claim 11, figure 1 shows that the buffering unit includes buffers (inverters) connected serial for receiving the confirmation signal.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikehashi et al. (USP 6642757).

Ikehasshi's figure 23 shows all limitations of the claims except for the resistors in the first and second power supply voltage detecting units are respectively PMOS transistor with gate connected to ground and NMOS transistor with gate connected to the supply voltage. However, it is notoriously well known in the art that PMOS transistor with gate connected to ground and NMOS transistor with gate connected to the supply voltage function as resistors. Therefore, it would have been obvious to one having ordinary skill in the art to use PMOS with gate connected to ground and NMOS with gate connected to the supply voltage for respective the resistors in the first and second power supply voltage detecting units for the purpose of saving space.

6. Claims 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Onishi (JP 2001-127609).

Onishi's figure 1 shows all limitations of the claims except for the resistors in the first and second power supply voltage detecting units are respectively PMOS transistor with gate

connected to ground and NMOS transistor with gate connected to the supply voltage. However, it is notoriously well known in the art that PMOS transistor with gate connected to ground and NMOS transistor with gate connected to the supply voltage function as resistors. Therefore, it would have been obvious to one having ordinary skill in the art to use PMOS with gate connected to ground and NMOS with gate connected to the supply voltage for respective the resistors in the first and second power supply voltage detecting units for the purpose of saving space.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quan Tra
Primary Examiner

April 18, 2005